REMARKS

The above amendments and following remarks are submitted under 37 C.F.R. 1.116 in response to the Final Official Action (i.e., Paper No. 14) of the Examiner mailed May 6, 2004. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Entry of this amendment and reconsideration to that end is respectfully requested.

Claims 1, 6-7, 11, 16, and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,850,534, issued to Kranich (hereinafter referred to as "Kranich") in view of U.S. Patent No. 6,247,094, issued to Kumar et al (hereinafter referred to as "Kumar"). This ground of rejection is respectfully traversed for the following reasons.

A key requirement of MPEP 2143 is that the alleged combination (i.e., Kranich in view of Kumar in this case) must contain all of the claimed limitations. Each of these claims (and indeed all pending claims) requires a dedicated path from the system bus to the level two cache tag storage which is separate from the path from the system bus to the level two cache data storage. The importance of this feature is found in Applicants' specification in numerous places including page 7, lines 13-18.

The Examiner admits that Kranich does not have this feature. However, he clearly erroneously states:

> Kumar discloses a data processing system for reducing cache latency wherein the improvement comprises a first dedicated path between a system bus and a cache storage [front side bus 190 communicates with L2 data array by means of line connected to way predictor 150; Fig. 7], and a second dedicated path between a system bus and a tag storage [front side bus 190 communicates with L2 tag array 135 by means of snoop queue line; Fig. 7]....

This statement is clearly erroneous because both L2 Tag Array 135 and L2 Data Array 120 communicate with Front Side Bus 190 via Bus Controller 130. This is in stark contrast to Applicants' claimed invention explained at page 14, lines 8-10, which states:

> Unlike prior art system controller[s], bus interface logic 60 provides separate and independent paths to ....

Though the Examiner has not presented the required evidence of "motivation" and "reasonable likelihood of success", the lack of all claim elements in the alleged combination is the most apparent. The rejection of claims 1, and 6-7, and all claims depending therefrom, is respectfully traversed.

Applicants have previously made this argument within Paper No. 13. To make this distinction even more explicit, Applicants have herewith amended all pending claims to indicate that these "separate and dedicated" paths specifically include "separate and dedicated" paths through the "system memory bus interface". This limitation is fully disclosed by Applicants in Fig. 4 and

accompanying discussion, particularly page 14, lines 7-10. This limitation is clearly not present in Kumar.

As if in agreement with Applicants' position, the Examiner states:

> Since (sic) the technology for implementing a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path was well known in the art and since a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path reduces cache latency by allowing the microprocessor to directly access the cache tag array without accessing the external bus during a lookup, an artisan would have been motivated to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via second dedicated path in the system of **Kumar**. (Emphasis added)

In other words, the Examiner states that It would be obvious to modify Kumar in accordance with Applicants' claimed invention (i.e., utilize separate and dedicated paths from the system bus to the data and tag memories). The Examiner then alleges that the combination of Kranich and Kumar would have all of the claimed elements. This logic is incorrect as a matter of law. MPEP 2143 specifically requires that the alleged combination itself (i.e., Kranich and Kumar) must contain all of the claimed limitations. It does not, and the Examiner admits that it does not. This ground of rejection is respectfully traversed.

With regard to the rejection of claims 2-5, 8-10, 12-15, 17-20, and 21-25, Applicants have already made arguments deemed sufficient in response to the Examiner's rejections. However,

because the Examiner has not properly considered the "dedicated and separate" coupling of data and tag memories, it is clear that he has not considered these additional arguments. Therefore, no purpose would be served by repeating these arguments until agreement is reached on the patentability of the claims from which they depend.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

Donald C. Englin et al.

By their attorney,

Date July 6, 2004

Wayne A. Sivertson
Reg. No. 25,645
Suite 401
Broadway Place East
3433 Broadway Street N.E.
Minneapolis, Minnesota
55413
(612) 331-1464